ABSTRACT OF THE INVENTION

[00100] There is disclosed a bus interface unit for transferring machine specific register (MSR) requests between a plurality of bus devices. The bus interface unit comprises: 1) a plurality of input ports for receiving incoming MSR requests from the plurality of bus devices; 2) a plurality of output ports for transmitting data to the plurality of bus devices; and 3) a controller for reading N routing associated with a first received MSR request and comparing a first identification (ID) value in a predetermined M-bit field in the N routing bits to a first designated value. The controller, in response to a determination that the first ID value does not equal the first designated value: 1) realigns the N routing bits such that remaining ones of the N-M bits outside the predetermined M-bit field are moved into the predetermined M-bit field and 2) transmits the realigned N routing bits via a first one of the plurality of output ports identified by the first ID value.